AKGEC-nI
LabVIEW Academy

PCI Express

Peripheral Component Interconnect Express, better known as PCI Express, was introduced to overcome the limitations of the original PCI bus. It uses a shared bus topology, where bus bandwidth is divided among multiple devices, to enable communication among the different devices on the bus. The most notable PCI Express advancement over PCI is its point-to-point bus topology.

Applications such as data acquisition and waveform generation require sufficient bandwidth to ensure that data can be transferred to memory fast enough without being lost or overwritten. With PCI Express data is streamed faster and the amount of required onboard memory is minimized. Using data storage technologies, such as RAID (Redundant Array of Independent Disks), large amounts of data produced by high-speed devices can be continuously streamed and stored for further analysis.

Features

- Communication consists of data and status-message traffic being packetized and depacketized.
- Data is sent via paired point-to-point serial links, called lanes, allowing data movement in both directions simultaneously and allowing more than one pair of devices to communicate simultaneously at 250 MB/s bandwidth per direction, per lane.
- PCI-E slots contain from one to 32 lanes in powers of 2 (1, 2,4, 8 etc.).
- Higher bandwidth is provided by channel grouping – using multiple lanes for a single device.
- Serial buses transmit data faster than parallel buses due to the latter limitation requiring data to arrive simultaneously at their destination (This has to do with the frequency and wavelength of a single bit).
- PCI-E follows a layered protocol composed of 3 layers: a transaction layer, a data link layer, and a physical layer.